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Development of SiC Epitaxial Wafer in WPM Program

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Abstract:

SiC is considered as the material for the next generation power semiconductors enabling the efficient power consumption in the future society. In Korea, the development of high purity SiC materials for power electronics started in 2010 under the national R&D program called WPM(World Premier Materials). LG Innotek has lead the project for the epitaxial wafer development and installed a hot wall single-wafer research reactor in 2011, the first one in Korea and a commercial scale reactor in 2016. The lowest background doping density of undoped epilayers was determined to be 1e14 cm-3. The n-type doping density of epilayers could be controlled between 5e15 cm-3 and 1e18 cm-3 by introducing high purity nitrogen gas. Typical defects observed in the epilayers were particles, triangles, carrots, stacking faults, and various types of dislocations. The formation of these defects, doping concentration, and epilayer thickness were connected by major process variables such as temperature, pressure, C/Si ratio, and gas flow in addition to the defects caused by the substrate quality. The process condition was optimized for defect reduction and uniformities of doping and thickness. Schottky barrier diodes and metal oxide semiconductor field effect transistors were fabricated on the epilayers to test their quality. Low cost process development will be the future improvement aiming for its commercialization.

Keywords

SiC, Epitaxial Wafer, WPM, Uniformity, Defect

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