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질화열처리를 통한 열산화막과 4H-SiC 계면의 전기적 특성 향상에 관한 연구

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Abstract:

Thermally nitrided oxide has been widely employed as gate oxide in 4H-SiC based metal-oxide-semiconductor (MOS) high power devices due to its low SiC-SiO_2 interface trap density (D_{it}). Majority of these works were performed at temperature lower than 1200 ℃. There are limited reports on the effect of nitrided oxide, both directly grown or post-oxidation annealed, at higher temperature. First, the HTO gate oxide was formed at 1350 ℃ for 27 min. in dry O_2 ambient, followed by NO POA at 1300 ℃ for 30 min. (oxide thickness ~ 57 nm). For comparison, a 55-nm-thick Pyrogenic Re-oxidized (PR) SiO_2 grown at 1150 ℃ was also prepared. After thermal gate oxide formation, NO POA treatments were performed at 1175 ℃ for 3 hours. The detailed description of the fabrication procedures for the MOS capacitors has been given elsewhere. The values of D_{it} for PR SiO_2 with NO POA was lower than that of the high temperature grown oxide at 1350 ℃ in dry O_2 ambient. Especially high temperature grown oxide at 1350 ℃ with NO POA at 1300 ℃ showed the lowest D_{it}. The measured D_{it} (at 0.3 eV, below the 4H-SiC conduction band edge) of high temperature grown oxide with NO POA was ~ 3.1×10^{10} $3cm^{-2}eV^{-1}$. The flatband voltage(V_{FB}) and effective oxide charge density(Q_{eff}) were significantly reduced by using the high temperature grown oxide at 1350 ℃ with NO POA at 1300 ℃ as compared with the value of the PR SiO_2 at 1150 ℃ that had underwent NO POA at 1175 ℃. On the other hand, the high temperature oxide grown at 1350 ℃ with NO POA at 1300 ℃ showed higher V_{FB} and Q_{eff} uniformity as compared with the values of PR SiO_2 with NO POA at 1175 ℃. This result suggests that NO POA at 1300 ℃ effectively improved the V_{FB}, Q_{eff} characteristics of the MOS capacitors. This result indicates that the D_{it} at SiO_2/SiC interface is controlled efficiently by HTO and NO POA at high temperature.

Keywords

Silicon Carbide, MOScapacitor, NO aneal, Gate Oxide

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